providing an attachment hole passing through ~~a~~ said board and through said interconnect pattern, ~~in a thickness direction~~ wherein said semiconductor device is mountable to said board with a connection terminal thereof over said attachment hole, and

press-fitting into said attachment hole a capacitor cable comprised of a conductor wire at the core, a high dielectric constant material coaxially covering the conductor wire ~~at a predetermined thickness~~, and a ~~conductor~~ conductive sheath covering the outer circumference of the high dielectric constant material ~~so at to attach the capacitor to said board~~, said conductive sheath being in press-fit electrical connection with said interconnect pattern,

wherein said core conductor wire is in position to be connected to said semiconductor device connection terminal positioned over said attachment hole.

4(currently amended) A method of production of a semiconductor package having a board to which a semiconductor device is mountable, said method mounting a capacitor for suppressing fluctuations of a ~~power supply~~ voltage in a wire connectable to said semiconductor device, comprising:

providing a grounded interconnect pattern on an inside layer of said board,

~~providing an attachment hole passing through a board in a thickness direction~~ making a hole passing through said board for passing a voltage wire to a said semiconductor device mounted to said board, said hole passing through said interconnect pattern and exposing said interconnect pattern at an inside wall thereof,

forming a ~~conductor~~ conductive layer ~~at an inner~~ on said inside wall of said ~~attachment~~ hole, said conductive layer being in contact with said exposed interconnect pattern, and

press-fitting into said ~~attachment~~ hole ~~formed with said layer a capacitor cable comprised of~~ a conductor wire for connection to said semiconductor device, ~~at the core and~~ said conductor wire having a high dielectric constant material coaxially covering the conductor wire,

~~at a predetermined thickness so as to attach the capacitor to said board~~ said dielectric material being in press fit contact with said formed conductive layer, wherein a capacitor is established with one element thereof being said conductor wire connectable to said semiconductor device and the other element thereof being conductive layer on said inside wall of said hole in press fit contact with said interconnect pattern .

5.(new) A method of connecting a capacitor in proximity to a connection terminal of a semiconductor device mountable to a printed circuit like board, comprising the steps of:

providing a grounded interconnect pattern on an inside layer of said board;

making an attachment hole through said board for passing a voltage connection wire there through to said semiconductor device, said hole extending though said interconnect pattern and exposing it at an inside wall of said hole;

passing a conductor wire through said hole for connection to said semiconductor device, said wire having voltage fluctuations thereon to be suppressed;

surrounding said voltage conductor wire with a coaxial thickness of high dielectric constant material; and

surrounding said high dielectric constant material with a outer coaxial conductive layer in press fit contact with said exposed interconnect pattern at said inside wall of said hole,

wherein a coaxial capacitor is established with one element being said voltage conductor wire to said semiconductor device and the other element being said outer conductive layer in press fit with said exposed interconnect pattern.

6. The method of claim 5, wherein said voltage conductor wire surrounding step includes coating conductor with a predetermined thickness of said high dielectric constant material, and wherein said dielectric material surrounding step includes surrounding said dielectric material

with a conductive sheath covering to form a capacitive cable, wherein said press fit contact is effected by press fitting said capacitive cable into said hole wherein said conductive sheath covering is in press fit contact with said exposed interconnect pattern at said inside wall thereof.

7.(new) The method of claim 5, wherein said voltage conductor wire surrounding step includes coating said conductor wire with a predetermined thickness of said high dielectric constant material, and wherein said dielectric material surrounding step includes coating said hole with a conductive layer, wherein said conductive layer is in contact with said exposed interconnect layer, and then press fitting said dielectric coated conductor wire into said conductive layer coated hole.

8.(new) The method of claim 7 wherein the step of coating said hole with a conductive layer is plating said hole with a conductive layer.